IN THE CLAIMS

Claims 1-14 (cancelled).

Claim 15 (currently amended): A high performance buffering technique for use with a serial peripheral interface to facilitate high data rates, said buffering technique comprising the steps of:

initializing a single buffer to act as transmitter and receiver by writing data to a data register;

performing a transmit buffering sequence to prepare for the transmitting of the data;

performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time; and

performing a receive buffering sequence to prepare for the receipt of additional new data.

Claim 16 (original): The high performance buffering technique of claim 15, wherein said initialization step comprises the step of:

writing the data into a location of said buffer as designated by a write pointer.

Claim 17 (original): The high performance buffering technique of claim 15, wherein said transmit buffering step comprises the steps of:

incrementing a write pointer to prevent a next byte to be transmitted from overwriting a previous written byte; and

incrementing a write shift counter to facilitate tracking of a number of bytes available for transmission.

Claim 18 (original): The high performance buffering technique of claim 15, wherein said transmit and receive shifting step comprises the steps of:

reading the data from a location in the buffer designated by a shift pointer;

writing the data to a transmit shift register;

shifting of the transmit shift register; and

receiving and storing the new data in a receive shift register in a location of said buffer designated by a read pointer.

Claim 19 (original): The high performance buffering technique of claim 15, wherein said receive buffering step comprises the steps of:

incrementing a shift pointer to identify a new location in the buffer for receiving data; and

incrementing a read shift counter to indicate that the new data has been received.

Claim 20 (original): The high performance buffering technique of claim 15, wherein said buffering technique further comprises the steps of:

interrupting a CPU if the data is ready for transmitting and said buffer is approximately full; and

interrupting the CPU if said buffer is ready to receive data and said buffer is approximately empty.

Claim 21 (original): A high performance buffering technique for use with a serial peripheral interface to facilitate high data rates, said buffering technique comprising the steps of:

indicating a location in a single buffer where a CPU can write data to be transmitted;

indicating a location in said single buffer where any received data can be stored for reading by the CPU;

indicating a location where data to be transmitted is located and a location where the received data will be stored after shifting of any registers is completed;

tracking a number of bytes of data that need to be transmitted; and

tracking a number of bytes of data that have been received.